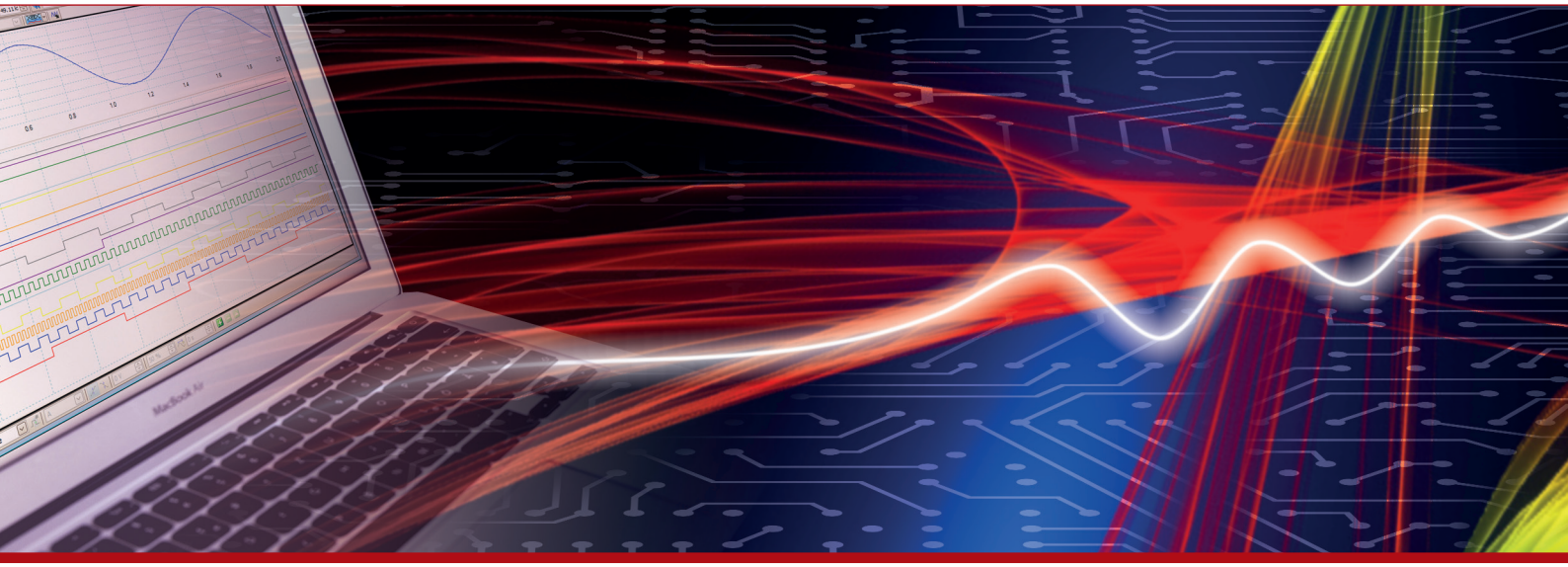
Product Datasheet - Technical Specifications



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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog voltage output

Table 1. Analog voltage output specifications

Parameter	Conditions	Specifications
Digital to Analog converter		DAC8554
Number of channels (Note 1)		4
Resolution		16 bits
Output ranges	Calibrated	±10 V, 0 to 10 V Software configurable
	Un-calibrated	±10.2 V, -0.04 to 10.08 V Software configurable
Output transient	±10 V to (0 to 10 V) or (0 to 10 V) to ±10 V range selection. (Note 2)	Duration: 5 uS typ. Amplitude: 5V p-p typ.
	Host PC is reset, powered on, suspended or a reset command is issued to device. (Note 3)	Duration: 2 S typ. Amplitude: 2V p-p typ.
	Initial power on	Duration: 50 mS typ. Amplitude: 5V peak typ.
Differential non-linearity (Note 4)	Calibrated	±1.25 LSB typ. -2 LSB to +1 LSB max.
	Un-calibrated	±0.25 LSB typ. ±1 LSB max.
Output current	VOUTx pins	±3.5 mA typ.
Output short-circuit protection	VOUTx connected to AGND	Indefinite
Output coupling		DC
Power on and reset state		DACs cleared to zero-scale: 0 V, ±50 mV typ.
		Output range: 0-10 V
Output noise	0 to 10 V range	14.95 µVrms typ.
	±10 V range	31.67 µVrms typ.
Settling time	*to 1 LSB accuracy*	*25 µS typ.*
Slew rate	0 to 10 V range	1.20 V/µS typ.
	±10 V range	1.20 V/µS typ.
Throughput	Single-channel	100 Hz max., system dependent
	Multi-channel	100 Hz/#ch max., system dependent

Note 1: Each of the four DAC8554 outputs controls a VOUTx and IOUTx channel-pair simultaneously. So, for example, when writing to channel VOUT0, the associated IOUT0 channel will also be updated. Conversely, when writing to channel IOUT0, the associated VOUT0 channel is also updated. Unused VOUTx and IOUTx output channels should be left disconnected.

Note 2: The RedLab 3102 output voltage level defaults to 0V whenever the output voltage range is reconfigured.

The RedLab 3102 output voltage level will also default to 0V:
1) Whenever the host PC is reset, shut down or suspended.
2) If a reset command is issued to the device.

Note 3: The duration of this particular output transient is highly dependent on the enumeration process of the host PC. Typically the output of the RedLab 3102 is stable after 2 seconds.

Note 4: The maximum differential non-linearity specification applies to the entire 0 to 50 °C temperature range of the RedLab 3102. This specification also accounts for the maximum errors due to the software calibration algorithm (in Calibrated mode only) and the DAC8554 digital to analog converter non-linearities.

Table 2. Absolute accuracy specifications – calibrated output

Range	Accuracy (±LSB)
±10 V	14.0
0 to 10 V	22.0

Table 3. Absolute accuracy components specifications – calibrated output

Range	% of reading	Offset (±mV)	Temp drift (%/°C)	Absolute accuracy at FS (±mV)
±10 V	±0.0183	1.831	0.00055	3.661
0 to 10 V	±0.0183	0.915	0.00055	2.746

Table 4. Relative accuracy specifications

Range	Relative accuracy (±LSB)	
±10 V , 0 to 10 V	4.0 typ.	12.0 max.

Analog current output

Table 5. Analog current output specifications

Parameter	Conditions	Specifications
Number of channels (Note 5)		4
Resolution		16 bits
Output ranges	Calibrated	0 to 20 mA typ.
	Uncalibrated	0 to 25 mA typ.
Compliance voltage range (Note 6)	Calibrated output	+8 V min. +36 V max.
Differential non-linearity (Note 7)	Calibrated	±1.25 LSB typ. -2 LSB to +1 LSB max.
	Un-calibrated	±0.25 LSB typ. -1 LSB to +1 LSB max.
Absolute accuracy	Compliance voltage = +13 V Resistive load = 100 Ω	±0.05% of full scale range
IOUTx leakage current	All zeros written to IOUTx channel	100 nA typ. (each individual IOUT channel)
Settling time	*Full scale step to 1LSB accuracy* *Compliance voltage = 12 V, Rload = 500 Ω*	*25 µS typ.*
Throughput	Single-channel	100 Hz max., system dependent

	Multi-channel	100 Hz/#ch max., system dependent

Note 5: Each of the four DAC8554 outputs controls a VOUTx and IOUTx channel-pair simultaneously. So, for example, when writing to channel VOUT0, the associated IOUT0 channel will also be updated. Conversely, when writing to channel IOUT0, the associated VOUT0 channel is also updated. Unused VOUTx and IOUTx output channels should be left disconnected.

Note 6: The following formula will calculate the maximum load resistance for correct IOUT circuit operation. The compliance voltage applied should not exceed the limits specified in Table 5.

- Calibrated Output:

  Load Resistance = (Compliance Voltage - 6V)/0.020A

- Un-Calibrated Output:

  Load Resistance = (Compliance Voltage - 6V)/0.025A

Note 7: The maximum differential non-linearity specification applies to the entire 0 to 70 °C temperature range of the RedLab 3102. This specification also accounts for the maximum errors due to the software calibration algorithm (in Calibrated mode only) and the DAC8554 digital to analog converter non-linearities.

Analog output calibration

Table 6. Analog output calibration specifications

Parameter	Conditions	Specifications
Recommended warm-up time		15 minutes min.
On-board precision reference		DC level: 5.000 V ±1 mV max.
		Tempco: ±10 ppm/°C max.
		Long term stability: ±10 ppm/SQRT(1000 hrs)
Calibration method		Software calibration
Calibration interval		1 year

Digital input/output

Table 7. Digital I/O specifications

Digital logic type	CMOS
Number of I/O	8
Configuration	Independently configured for input or output
Pull-up/pull-down configuration (Note 8)	User configurable All pins floating (default)
Digital I/O input loading	TTL (default)
	47K ohms (pull-up/pull down configurations)
Digital I/O transfer rate (system paced)	System dependent, 33 to 1000 port reads/writes or single bit reads/writes per second.
Input high voltage	2.0 V min, 5.5 V absolute max
Input low voltage	0.8 V max, –0.5 V absolute min
Output high voltage (IOH = –2.5 mA)	3.8 V min
Output low voltage (IOL = 2.5 mA)	0.7 V max
Power on and reset state	Input

Note 8: Pull up and pull down configuration area available using the DIO CTL terminal block pin 54. The pull down configuration requires the DIO CTL pin (pin 54) to be connected to a DGND pin (pin 50, 53 or 55). For a pull up configuration, the DIO CTL pin should be connected to the +5V terminal pin (pin 56).

Synchronous DAC Load

Table 8. SYNCLD I/O specifications

Parameter	Conditions	Specification
Pin name		SYNCLD (terminal block pin 49)
Power on and reset state		Input
Pin type		Bidirectional
Termination		Internal 100K ohms pull-down
Software selectable direction	Output	Outputs internal D/A LOAD signal.
	Input	Receives D/A LOAD signal from external source.
Input clock rate		100 Hz max
Clock pulse width	Input	1 µs min
	Output	5 µs min
Input leakage current		*±1.0 µA typ.*
Input high voltage		4.0 V min, 5.5 V absolute max
Input low voltage		1.0 V max, –0.5 V absolute min
Output high voltage (Note 9)	IOH = –2.5 mA	3.3 V min
	No load	3.8 V min
Output low voltage (Note 10)	IOL = 2.5 mA	1.1 V max
	No load	0.6 V max

Note 9: SYNCLD is a Schmitt trigger input and is over-current protected with a 200 Ohm series resistor.

Note 10: When SYNCLD is in input mode, the analog outputs may either be updated immediately or when a positive edge is seen on the SYNCLD pin (this is under software control.) However, the pin must be at a low logic level in order for the DAC outputs to be updated immediately. If an external source is pulling the pin high, no update will occur.

Counter

Table 9. CTR I/O specifications

Parameter	Conditions	Specification
Pin name		CTR
Number of channels		1
Resolution		32-bits
Counter type		Event counter
Input type		TTL, rising edge triggered
Counter read/writes rates (software paced)	Counter read	System dependent, 33 to 1000 reads per second.
	Counter write	System dependent, 33 to 1000 reads per second.
Schmidt trigger hysteresis		20 mV to 100 mV
Input leakage current		*±1.0 µA typ.*
Input frequency		1 MHz max.
High pulse width		*500 nS min.*
Low pulse width		*500 ns min.*
Input high voltage		4.0 V min, 5.5 V absolute max
Input low voltage		1.0 V max, –0.5 V absolute min

Memory

Table 10. Memory specifications

EEPROM	256 bytes		
EEPROM configuration	**Address range**	**Access**	**Description**
	0x000-0x0FF	Read/write	256 bytes user data

Microcontroller

Table 11. Microcontroller specifications

Type	*High performance 8-bit RISC microcontroller*
Program memory	*16,384 words*
Data memory	*2,048 bytes*

Power

Table 12. Power specifications

Parameter	Conditions	Specification
Supply current	USB enumeration	< 100 mA
Supply current (Note 11)	Quiescent current	140 mA typ.
+5V user output voltage range (Note 12)	Available at terminal block pin 56	4.5 V min, 5.25 V max.
+5V user output current (Note 13)	Available at terminal block pin 56	10 mA max.
ITEST output voltage range	Available at terminal block pin 51	13V, ±1% typ.
ITEST output current (Note 14)	Available at terminal block pin 51	30mA max.

Note 11: This is the total quiescent current requirement for the RedLab 3102 which includes up to 10 mA for the status LED. This does not include any potential loading of the digital I/O bits, +5V user terminal, ITEST, or the VOUTx/IOUTx outputs.

Note 12: Output voltage range assumes USB power supply is within specified limits.

Note 13: This refers to the total amount of current that can be sourced from the +5V user terminal (pin 56) for general use. This specification also includes any additional contribution due to DIO loading.

Note 14: This refers to the total maximum amount of current that can be sourced from the ITEST user terminal (pin 51). The ITEST terminal pin should only be used for biasing individual IOUTx outputs in order to facilitate functional testing. A load resistor of 100Ω should be placed in series between the ITEST pin and the IOUTx pin for proper operation.

USB specifications

Table 13. USB specifications

USB device type	USB 2.0 (full-speed)
USB device compatibility	USB 1.1, 2.0
USB cable length	3 meters max.
USB cable type	*A-B cable, UL type AWM 2527 or equivalent (min 24 AWG VBUS/GND, min 28 AWG D+/D-).*

Environmental

Table 14. Environmental specifications

Operating temperature range	0 to 50 °C
Storage temperature range	-40 to 85 °C
Humidity	0 to 90% non-condensing

Mechanical

Table 15. Mechanical specifications

Dimensions	127 mm (L) x 88.9 mm (W) x 35.56 (H)

Main connector and pin out

Table 16. Main connector specifications

Connector type	Screw terminal
Wire gauge range	16 AWG to 30 AWG

Pin	Signal Name	Pin	Signal Name
1	VOUT0	29	VOUT1
2	IOUT0	30	IOUT1
3	VOUT2	31	VOUT3
4	IOUT2	32	IOUT3
5	AGND	33	AGND
6	NC	34	NC
7	NC	35	NC
8	NC	36	NC
9	NC	37	NC
10	AGND	38	AGND
11	NC	39	NC
12	NC	40	NC
13	NC	41	NC
14	NC	42	NC
15	AGND	43	AGND
16	NC	44	NC
17	NC	45	NC
18	NC	46	NC
19	NC	47	NC
20	AGND	48	AGND
21	DIO0	49	SYNCLD
22	DIO1	50	DGND
23	DIO2	51	ITEST
24	DIO3	52	CTR
25	DIO4	53	DGND
26	DIO5	54	DIO CTL
27	DIO6	55	DGND
28	DIO7	56	+5V